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AN10010

ISP1181A/ISP1181B/ISP1183 Frequently Asked Questions

Rev. 05 — 27 November 2007 Application note

Document information

Info	Content
Keywords	isp1181a, isp1181b, isp1183; faq, usb
Abstract	This document is a compilation of Frequently Asked Questions (FAQs) on NXP Universal Serial Bus Peripheral Controllers at full-speed: ISP1181A, ISP1181B and ISP1183.

founded by Philips

Revision history

Rev	Date	Description
05	20071127	Fifth release. Updated Section 2.8.
04	20071106	Fourth release. Added Section 7.4.
03	20070206	Third release. Added the ISP1183, wherever applicable. Updated Section 7.3. Added Section 2.8 and Section 2.9.
02	20040414	Updated Section 4.5; Changed terminology of “interface device” and “device controller” to “peripheral controller”.
01	20020301	First release.

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1. General product information

1.1 What are the differences between the ISP1181A/ISP1181B/ISP1183 and the PDIUSBD12?

The ISP1181A/ISP1181B/ISP1183 is a high-end Universal Serial Bus (USB) Peripheral Controller that complies with *Universal Serial Bus Specification Rev. 2.0*, supporting data transfer at full-speed (12 Mbit/s). It offers a generic parallel interface with faster access speed than the PDIUSBD12, enabling you to connect it to any high-speed microcontroller or RISC processor. Table 1 lists major differences between the PDIUSBD12 and the ISP1181A/ISP1181B/ISP1183.

Table 1. Characteristic differences between the PDIUSBD12 and the ISP1181A/ISP1181B/ISP1183

Characteristics	PDIUSBD12	ISP1181A/ISP1181B	ISP1183
Generic parallel interface	8-bit	8-bit or 16-bit	8-bit
Interface	2 Mbyte/s	11.1 Mbyte/s	11.1 Mbyte/s
Physical FIFO memory size	312 bytes	2462 bytes	2462 bytes
Number of endpoints	6 endpoints (including control IN and OUT)	14 configurable endpoints and 2 fixed control IN/OUT	14 configurable endpoints and 2 fixed control IN/OUT

1.2 Is the ISP1181A/ISP1181B/ISP1183 compliant with USB 2.0?

The ISP1181A/ISP1181B/ISP1183 is used only as the physical layer and basic protocol layer interface. It is compliant with *Universal Serial Bus Specification Rev. 2.0* (full-speed).

2. Interfacing

2.1 What is the use of the V_{BUS} sensing input pin?

V_{BUS} is the 5 V power supply pin from the USB connector. The ISP1181A/ISP1181B has a separate input pin to detect the presence of V_{BUS}. In a self-powered system, the ISP1181A/ISP1181B detects the removal of the USB cable through the V_{BUS} input pin. When V_{BUS} is lost, the ISP1181A/ISP1181B prepares itself to enter the ‘suspend’ state. The GOSUSP bit in the Mode register must first be set and then cleared to set the device to suspend. This changes the state of the SUSPEND output pin. The behavior of the SUSPEND output depends on the PWROFF bit in the Hardware Configuration register.

In a self-powered system with an internal pull-up resistor (SoftConnect), when the host is powered down, V_{BUS} is lost. The chip automatically disables the internal pull-up resistor of 1.5 kΩ. This prevents any current flow from the device to the host. The detection of V_{BUS} is done by the V_{BUS} sensing pin.

In a self-powered system with an external pull-up resistor, when the host is powered down, the external pull-up resistor will still pull D+ to HIGH. This causes current to flow from the device to the host. Designers must design a workaround circuit to prevent this current flow. There will be no such issues if you use the internal pull-up resistor.

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2.2 What is the use of the $V_{reg(3.3)}$ pin?

The $V_{reg(3.3)}$ pin allows a regulated voltage supply of 3.3 V to the 1.5 kΩ pull-up resistor. You can, however, use the internal SoftConnect resistor instead. It is recommended that you do not load this pin, other than with the 1.5 kΩ resistor.

2.3 How does EOT work in ISP1181A/ISP1181B?

The End-Of-Transfer (EOT) signal terminates the DMA transfer. In the ISP1181A/ISP1181B, the DMA transfer can be terminated in the following ways:

- External EOT signal.
- Internal DMA counter completes its count (when the DMA Counter register is enabled).
- DMA transfer finishes a short packet received on the OUT endpoint FIFO (when the short packet mode is enabled).

Disable DMA by writing DMAEN = 0 to the DMA Configuration register.

Remark: There will be no interrupt to indicate EOT.

All the preceding conditions are recognized by the ISP1181A/ISP1181B as EOT conditions.

If the external DMA controller must terminate the DMA transfer, it can perform an external EOT by sending the signal to the EOT pin on the ISP1181A/ISP1181B. The remaining three EOT conditions are caused internally.

If an OUT endpoint FIFO is selected for the DMA transfer and there are data bytes remaining in the FIFO when the EOT condition occurs, the DMA operation is aborted and the remaining data in the FIFO is cleared. (For a double-buffered endpoint, the data packet contained in another buffer is not affected by the current EOT). If an IN endpoint FIFO receives an EOT condition, the data packet that is written to the FIFO, even shorter than the maximum packet size of the FIFO, will be sent to the host at the next IN token.

Typically, the transfer byte count must be set using a control endpoint before any DMA transfer takes place. When a short packet is enabled as an EOT indicator (SHORTP = 1), the transfer size is determined by the presence of a short packet in data. This mechanism permits the use of a fully autonomous data transfer protocol.

2.4 What are bus configurations and interfaces possible on the ISP1181A/ISP1181B?

To cater for various microcontrollers and microprocessors, the ISP1181A/ISP1181B allows versatile interface configurations. Bus configuration modes are selected using two pins, BUS_CONF1 and BUS_CONF0, see Table 2.

Table 2. Bus mode configuration

Mode	BUS_CONF[1:0]	PIO data width	DMA data width (DMAWD = 0)	DMA data width (DMAWD = 1)
0	00	DATA[15:0]	-	DATA[15:0]
1	01	reserved	reserved	reserved
2	10	DATA[7:0]	DATA[7:0]	-
3	11	reserved	reserved	reserved

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Mode 0: The 16-bit I/O port is shared with the 16-bit DMA port.

Mode 2: The 8-bit I/O port is shared with the 8-bit DMA port.

2.5 How do input pins A0 and ALE function in the ISP1181A/ISP1181B?

Input pin A0 functions as an address input pin. It selects a command when A0 = 1 and data when A0 = 0. In the multiplexed address and data bus configuration (that is, when input pin AD functions as address A0 as well as bit 0 of DATA[15:0]), input pin A0 is not used and must be connected to GND (LOW).The multiplexed address and data configuration works with reference to input pin ALE.

In a separate address and data bus configuration, the ALE pin must be connected to GND (LOW). When the ALE pin is in use, it goes through these phases:

- Address phase: A HIGH-to-LOW transition on the ALE pin latches the level on this pin as address A0 (1 = command, 0 = data).
- Data phase: During reading, this pin outputs bit DATA[0]; during writing, the level on this pin is latched as DATA[0].

2.6 Does the ISP1181A/ISP1181B operate with a 5.0 V or 3.3 V input?

The ISP1181A/ISP1181B can take either a 5.0 V or 3.3 V input. To operate the ISP1181A/ISP1181B at 5.0 V, connect the V_{CC} pin to supply voltage 5.0 V and connect the other supply pins as shown in Fig 1 (with decoupling capacitors).

To operate the ISP1181A/ISP1181B at 3.3 V, connect the supply voltage to the V_{CC}, $V_{CC(3.3)}$, V_{ref} and $V_{reg(3.3)}$ pins along with a decoupling capacitor. This connection is as shown in Fig 2.

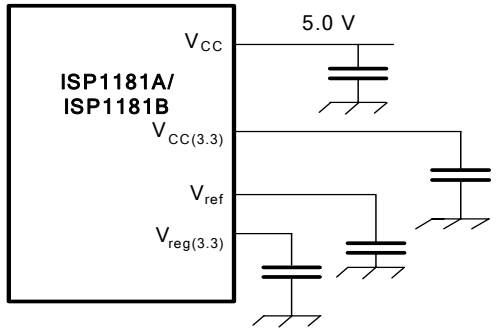

Fig 1. ISP1181A/ISP1181B with a 5.0 V supply

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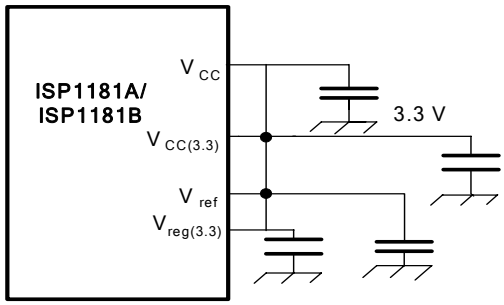

Fig 2. ISP1181A/ISP1181B with a 3.3 V supply

2.7 What is the fastest speed achievable on the parallel interface in the ISP118BA/ISP118B?

In the 8-bit configuration, the minimum read/write cycle time is 90 ns, which amounts to a transfer speed of 11.1 Mbyte/s. For each read operation, the read pulse ($\overline{RD}$) must be held LOW for a minimum of 25 ns. For each write operation, the write pulse must be held LOW for a minimum of 22 ns.

While interfacing to any high-speed microcontrollers or RISC processors, ensure that the read and write pulse width, and the read and write cycle time are taken into account. Add sufficient delays between two consecutive read and write in the firmware if the transfer speed of the microcontroller or the RISC processor is faster than the ISP1181A/ISP1181B.

2.8 How can the ISP1181A/ISP1181B enter test mode?

When the RESET_N pin is LOW, ensure that the A0 and CS_N pins are not toggling. Otherwise, the device will enter test mode.

To exit test mode, you must power down and restart the device.

2.9 How can the ISP1183 enter test mode?

When the RESET_N pin is LOW, ensure that the DACK and WAKEUP pins are LOW. Otherwise, the device will enter test mode.

To exit test mode, you must power down and restart the device.

3. Clocking

3.1 What is the crystal type to be used for ISP1181A/ISP1181B/ISP1183?

A 6 MHz-to-48 MHz clock multiplier Phase-Locked Loop (PLL) is integrated on-chip. This allows the use of a low-cost 6 MHz (fundamental) crystal. This low value minimizes EMI. Table 3 shows the characteristics of the crystal that must be used in the ISP1181A/ISP1181B/ISP1183.

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Table 3. Characteristics of the crystal used for the ISP1181A/ISP1181B/ISP1183

Characteristics	Value	Remarks
Nominal frequency	6 MHz	Fundamental
Frequency temperature stability	±50 ppm	–20 °C to +70 °C
Frequency tolerance	±50 ppm	+25 °C
Equivalent series resistance	< 100 Ω	-
Load capacitance	18 pF	-
Shunt capacitance	< 7 pF	-
Operating temperature range	–10 °C to +70 °C	-
Storage temperature range	–45 °C to +80 °C	-
Maximum drive level	0.1 mW (max.)	-

4. Suspend

4.1 When does the ISP1181A/ISP1181B/ISP1183 enter the ‘suspend’ state?

The ISP1181A/ISP1181B/ISP1183 detects the ‘suspend’ state in these three ways:

- A continuous J-state is present on the USB bus for more than 3 ms.
- V_{BUS} is lost.
- SoftConnect is disabled by clearing the SOFTCT bit in the Mode register, with the external pull-ups disabled by setting EXTPUL = 0 in the Hardware Configuration register. In this situation, the ISP1181A/ISP1181B/ISP1183 is effectively disconnected from the USB bus.

Any of these three conditions will make the ISP1181A/ISP1181B/ISP1183 initiate the SUSPEND process. This will set the SUSPND bit in the Interrupt register and will generate an interrupt (provided the IESUSP bit in the Interrupt Enable register is set).

4.2 How does the ISP1181A/ISP1181B/ISP1183 enter suspend mode after detecting the ‘suspend’ condition?

On detecting the ‘suspend’ condition, the ISP1181A/ISP1181B/ISP1183 sets the SUSPND bit in the Interrupt register, which in turn generates the interrupt. Therefore, the firmware detects the ‘suspend’ condition and prepares all system components to enter the ‘suspend’ state.

In the interrupt service routine, before initiating the ‘suspend’ state, the firmware must check the current status of the USB bus. If the BUSTATUS bit in the Interrupt register is logic 0, it indicates that the USB bus has left the ‘suspend’ state and the ‘suspend’ process must be aborted. Otherwise, the firmware will continue the process by first setting the GOSUSP bit in the Mode register and then clearing the bit. Once this is done, the ISP1181A/ISP1181B/ISP1183 asserts the SUSPEND output and switches off the internal clocks after 2 ms (depending on the setting of the CLKRUN bit in the Hardware Configuration register). The behavior of the SUSPEND output depends on the PWROFF bit set in the Hardware Configuration register.

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For bus-powered devices, to meet the stringent current requirements for the ‘suspend’ state, internal clocks must be switched off by clearing the CLKRUN bit in the Hardware Configuration register.

4.3 How does the ISP1181A/ISP1181B/ISP1183 resume from the ‘suspend’ state?

The ISP1181A/ISP1181B/ISP1183 wakes up from the ‘suspend’ state either by initiating the USB host or by the application.

- USB host: When the host drives the K-state on the USB bus (global resume), or when there is bus activity on the USB bus.
- Application: Remote wake-up through a HIGH level on input pin WAKEUP or a LOW level on input pin $\overline{CS}$ (wake-up on chip select is possible if the WKUPCS bit in the Hardware Configuration register is enabled).

4.4 What is the purpose of the ‘Unlock Device’ command?

During the ‘suspend’ state, in a powered-off application, the power supply to the CPU and the other parts are cut off. Input pins are pulled to ground through pin buffers. Outputs are in 3-state to prevent current flowing in the application. Bidirectional pins are made 3-state (must be externally pulled to ground by the application). It is possible that interface signals $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ have unknown values immediately after leaving the ‘suspend’ state because external components are also powered off. The uncertain value of these signals may corrupt internal registers immediately after enabling the ‘suspend’ state. Therefore, to prevent corruption, the ISP1181A/ISP1181B/ISP1183 enables a locking mechanism once the ‘suspend’ state is enabled.

After waking up from the ‘suspend’ state, all internal registers, except the Unlock register, are write-protected. A special unlock operation (using the Unlock Device command) is required to re-enable the write access to prevent data corruption during power-up of external components.

4.5 How can the SUSPEND pin be used for a powered-off application in relation with the PWROFF bit in the ISP1181A/ISP1181B?

The power-on state of the PWROFF bit is logic 0. This corresponds to a HIGH level on the SUSPEND pin when the Peripheral Controller is not in suspend mode. The PWROFF bit must be programmed to logic 1 that corresponds to a LOW level on the SUSPEND pin when a Peripheral Controller is not in suspend. See Fig 3 and Table 4.

- This workaround assumes that the default state of microprocessor GPIO is LOW.
- Microprocessor GPIO is LOW also after a reset.
- After initialization of the Peripheral Controller, the SUSPEND pin of the Peripheral Controller will typically become LOW.
- On receiving the suspend change interrupt from the Peripheral Controller, the microprocessor suspends the Peripheral Controller through the Mode register. This results in the SUSPEND pin of the Peripheral Controller going HIGH.
- Before the microprocessor enters low-power mode, the microprocessor sets the wake-up detection circuit by setting the GPIO pin HIGH and suspending itself.
- When wake up occurs, suspend becomes LOW and is inverted using an inverter. The GPIO and inverted suspend signals will go through an AND operation, followed by an inverter to reset the microprocessor.

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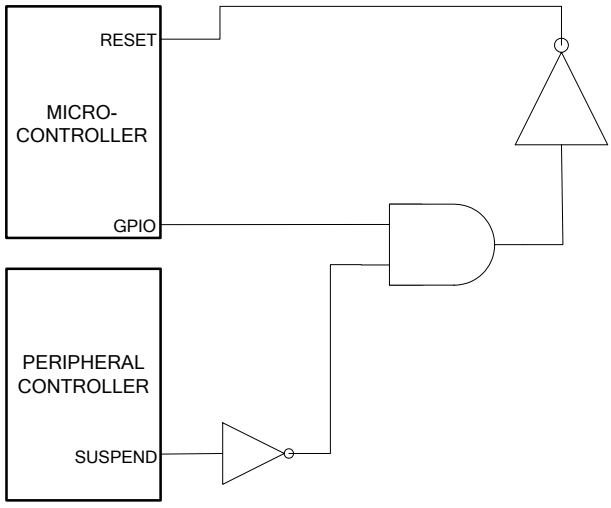

Fig 3. Block diagram

Table 4. Truth table

State	SUSPEND pin	!	GPIO	Reset	!
Default state	1	0	0	0	1
Init DC PWROFF = 1	0	1	0	0	1
Suspend	1	0	0	0	1
ARM (GPIO)	1	0	1	0	1
Wake up	0	1	1	1	0
After microprocessor reset	0	1	0	0	1

Remark: The circuit depends on de-assertion of GPIO to bring the microprocessor out of the suspend state. If the microprocessor resets or de-asserts GPIO during the LOW-level portion of the reset pulse (refer to dashed line A in Fig 4), the microprocessor will come out of the reset state. If the microprocessor was looking for the rising edge of the reset pulse to reset or de-assert GPIO (refer to dashed line B in Fig 4), the microprocessor will stay in a constant reset state. Therefore, the expected behavior of the microprocessor should be as shown at dashed line A. The application will not function if the behavior of the microprocessor is as shown at dashed line B.

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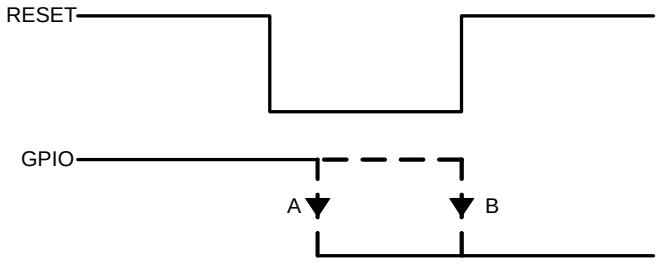

Fig 4. Reset of GPIO with respect to microprocessor

5. Others

5.1 What is the internal buffer size of the ISP1181A/ISP1181B/ISP1183?

The integrated physical buffer size is 2462 bytes, which is shared among all the enabled USB endpoints. The size of the 14 endpoints can independently be configured through the Endpoint Configuration register, but the total physical size of all the enabled endpoints must not exceed 2462 bytes.

5.2 What is double buffering?

Double buffering allows data to be OUT or IN on the USB bus while the internal buffer is still being read or written by the microcontroller or the DMA controller. This feature increases the overall throughput because the host does not have to wait for the internal buffer to be cleared or filled before feeding or extracting the next packet.

In the ISP1181A/ISP1181B/ISP1183, double buffering is possible on all the 14 endpoints.

Double buffering can be enabled or disabled by setting the DBLBUF bit in the Endpoint Configuration register (in device PDIUSBD12 double buffering is always enabled). Remember the physical size (2462 bytes) when allocating FIFO sizes for the double buffering feature for each endpoint.

5.3 What is GoodLink in ISP1181A/ISP1181B?

Indication of a good USB connection is provided at pin $\overline{GL}$ through the GoodLink technology. During enumeration, the LED indicator will momentarily blink. When the ISP1181A/ISP1181B has successfully been enumerated (the device address is set), the LED indicator will remain permanently on. During each successful packet transfer, the LED will blink off for 100 ms. During the ‘suspend’ state, the LED will remain in the off condition.

This feature provides a user-friendly indication on the status of the USB device, the connected hub and the USB traffic.

The LED can be connected to the $\overline{GL}$ pin (open drain, 8 mA) as shown in Fig 5. When supply voltage V_{CC} is 5.0 V, recommended series resistor ‘R’ must be 560 Ω. If the supply voltage V_{CC} is 3.3 V, then series resistor ‘R’ can be 330 Ω.

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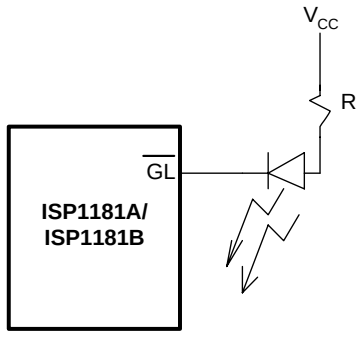

Fig 5. Connection of LED to the $\overline{GL}$ pin

5.4 What is SoftConnect?

You can enable the SoftConnect feature by using the SOFTCT bit in the Mode register. The SOFTCT bit is directly connected to the pull-up resistor on the D+ USB line. (The SOFTCT bit is ignored if the EXTPUL bit is set to logic 1 in the Hardware Configuration register). Setting the SOFTCT bit in the Mode register will enable the pull-up resistor of 1.5 kΩ that is required for the device detection. Therefore, the host or the hub will detect that something is plugged onto its USB port even though it was physically connected before setting up the SOFTCT bit.

SoftConnect allows the microcontroller or the processor to finish its initialization process before it notifies the host of its presence. This is especially valuable in a bus-powered device where the 5 V power supply must be stable before the enumeration. Besides, the USB connect or disconnect scenario can be created by setting or clearing bit SOFTCT. This forces the host to do a re-enumeration and reload the host device driver. This allows a device initiated upgrade without requiring you to physically disconnect and connect the USB cable.

6. Power up

6.1 How does the POR circuit work in the ISP1181A/ISP1181B/ISP1183?

The ISP1181A/ISP1181B/ISP1183 has an internal Power-On Reset (POR) circuitry. Therefore, the $\overline{RESET}$ pin can directly be connected to V_{CC}. A POR is automatically generated when V_{CC} goes below the trigger voltage of 2.0 V for a duration longer than 50 µs.

6.2 When is device ISP1181A/ISP1181B/ISP1183 accessible after power-on?

The clock signal starts about 0.5 ms after power-on and it typically requires 3 ms to 4 ms to stabilize. Therefore, it is better to start accessing the ISP1181A/ISP1181B/ISP1183 5 ms after power-on.

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7. Design considerations

7.1 What are the basic design considerations that must be taken into account?

Some basic PCB design guidelines are:

- Try to maintain the D+ and D– lines equal in length and width. It is better to keep the length of the D+ and D– lines traces to the USB connector as short as possible.
- Keep the crystal oscillator very close to device ISP1181A/ISP1181B/ISP1183. Keep the traces connecting to XTAL1 and XTAL2 of the ISP1181A/ISP1181B/ISP1183 as short as possible. Also, the two traces must be guarded with ground lines.
- Keep the V_{CC} and GND signals as thick as possible. They must never be less than 20 mils (0.5 mm) in thickness.

7.2 What are the EMI issues that must be taken into account?

EMI and EFT issues are too broad to be covered here. Here are some guidelines:

- In general, ferrite beads can be added on V_{BUS} and GND at the input side of the USB connector. The recommended ferrite bead part number is BLM32A07.
- It is a good practice to have capacitive coupling from the USB shield to the electrical ground.

7.3 How to suppress noise on the USB bus?

The USB bus performs differential transmission of signals. *Universal Serial Bus Specification Rev. 2.0* supports three transmission modes: 1.5 Mbit/s, 12 Mbit/s and 480 Mbit/s, of which the ISP1181A/ISP1181B/ISP1183 supports 12 Mbit/s (full-speed).

It is very important to suppress noise without distorting signals, and it is necessary to match the noise suppression to transmission mode.

Here are some basic guidelines:

- Add common-mode choke coil PLP3216S221SL2 (220 Ω at 100 MHz, 100 mA) on the D+ and D– lines.

or

- Add ferrite bead BLM11B102S on the D+ and D– lines.

These values must be used only as a guideline. Actual values will vary depending on the PCB design, components, and so on. In addition, when choosing ferrite beads and choke coils, ensure that proper impedance values are chosen for the design. For example, a larger impedance value has better noise suppression. Unfortunately, it has a severe effect on the signal quality.

7.4 What are the recommended ESD diodes for use with the ISP1181A/ISP1181B/ISP1183?

To protect the ISP1181A/ISP1181B/ISP1183 IC, we suggest that you use NXP IP4359 or IP4221CZ6-S.

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8. Abbreviations

Table 5. Abbreviations

Acronym	Description
DMA	Direct Memory Access
EFT	Electrical Fast Transient
EMI	ElectroMagnetic Interference
EOT	End-Of-Transfer
FIFO	First In, First Out
GPIO	General Purpose Input/Output
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POR	Power-On Reset
RISC	Reduced Instruction Set Code
USB	Universal Serial Bus

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