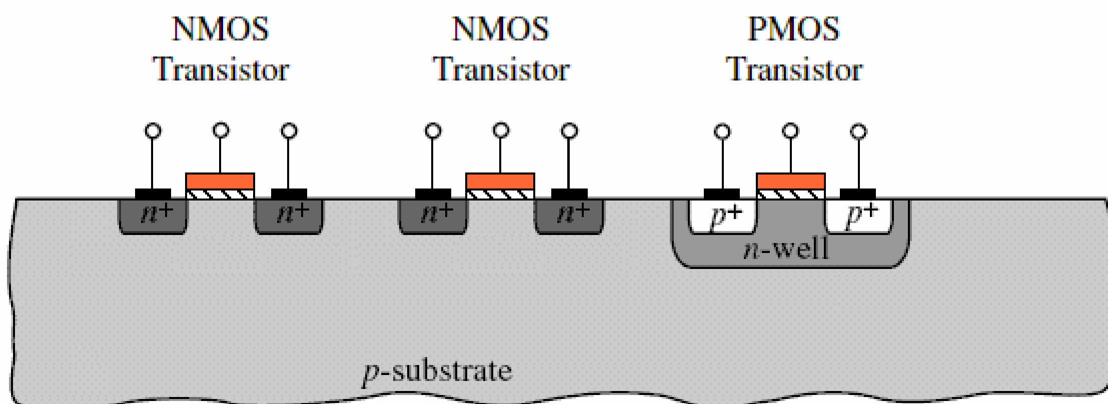
BASIC CMOS TECHNOLOGY

Illustration of a typical CMOS process:

- p-substrate
- n-well technology
- one or two polysilicon level
- up to eight metal level (Al o Cu) [*not shown*]

Structures:

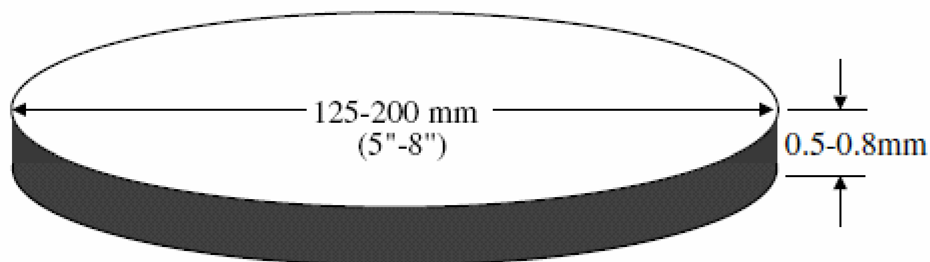
- NMOS/PMOS
- BJT (lateral)
- Capacitors
- Resistors



Basic steps:

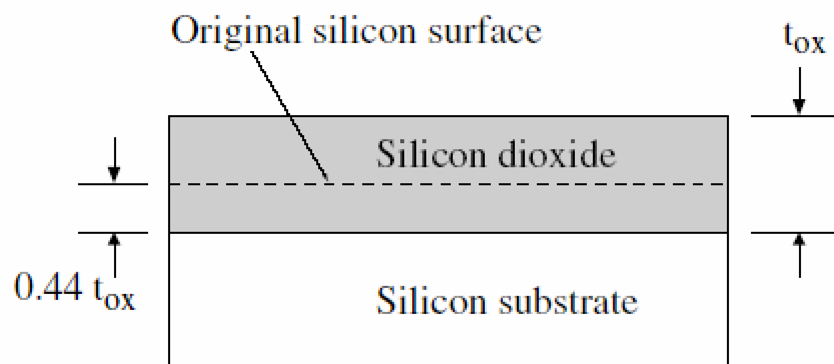
- Oxide growth
- Doping (*diffusion, ion implantation*)
- Deposition (*metal, polysilicon*)
- Etching
- *(Epitaxy)*

Silicon Wafer:



Oxidation

Oxidation is the process by which a layer of silicon is grown on the surface of a silicon wafer



Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers

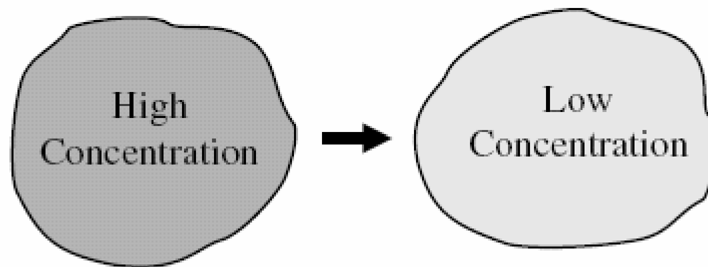
Oxidation techniques:

- dry (very thin and precise oxides, 100Å to 1000Å)
- wet (thick oxides, > 1000Å)

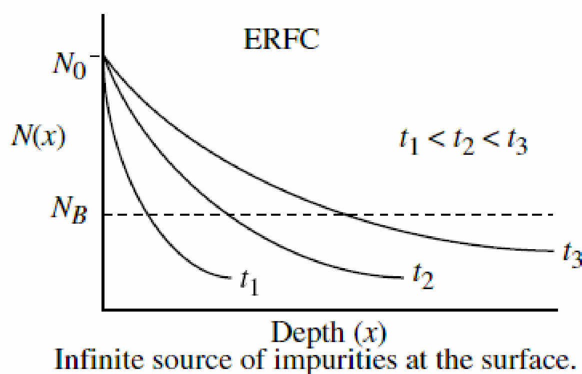
Doping

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

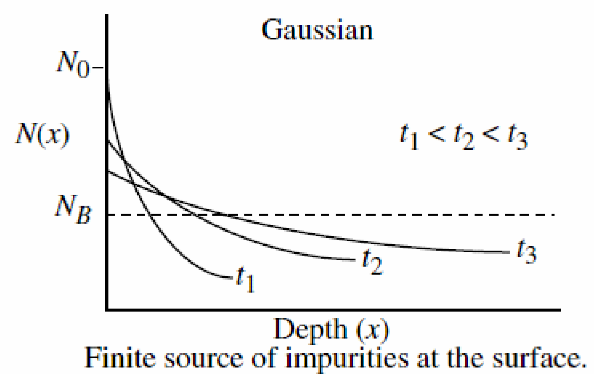
Always in the direction from higher concentration to lower concentration!!



Diffusion is done typically ay very high temperatures! (800°C to 1400°C)

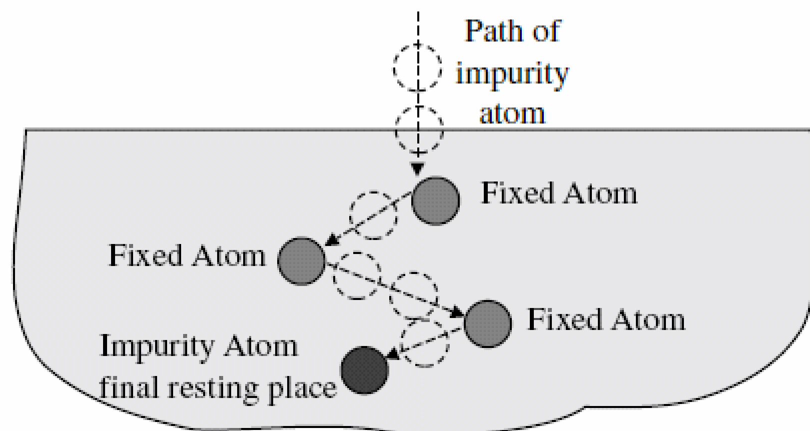


Infinite source of impurities at the surface.



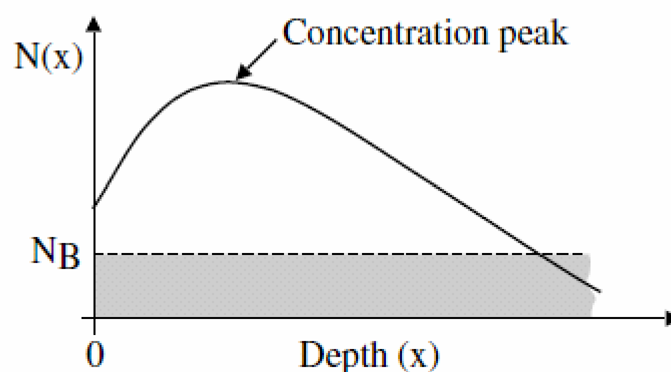
Finite source of impurities at the surface.

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material



- Annealing is required to repair the physical damage to the crystal lattice. This step is done at 500℃ to 800℃.

- Can achieve unique doping profile such as buried concentration peak.



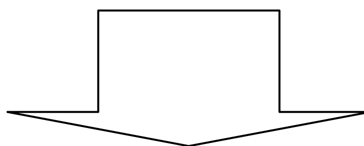
Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon

The deposition is typically made through a chemical-vapor deposition (CVD)

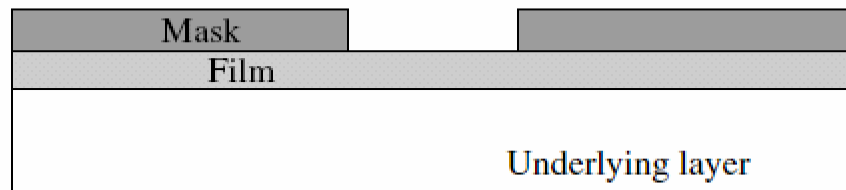
IMPORTANT: Materials that is being deposited covers the entire wafer



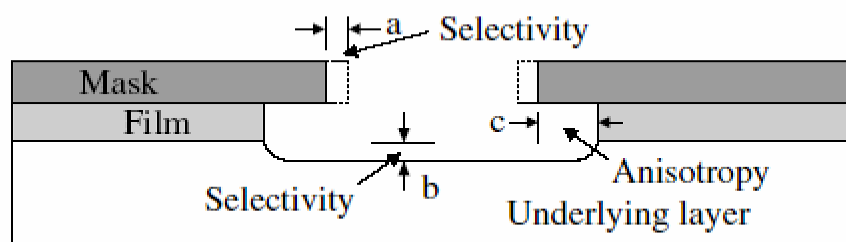
Etching is necessary!!!!!

Etching

Etching is the process of selectively removing a layer of material



(a) Portion of the top layer ready for etching.



(b) Horizontal etching and etching of underlying layer.

Important consideration:

- Anisotropy
- Selectivity

So, when etching is performed, the etchant may remove portions or all of

- The desired material
- The underlying layer
- The masking layer

Photolithography

Photolithography is the process of transferring geometric shapes on a mask to the surface of a silicon wafer.

Components:

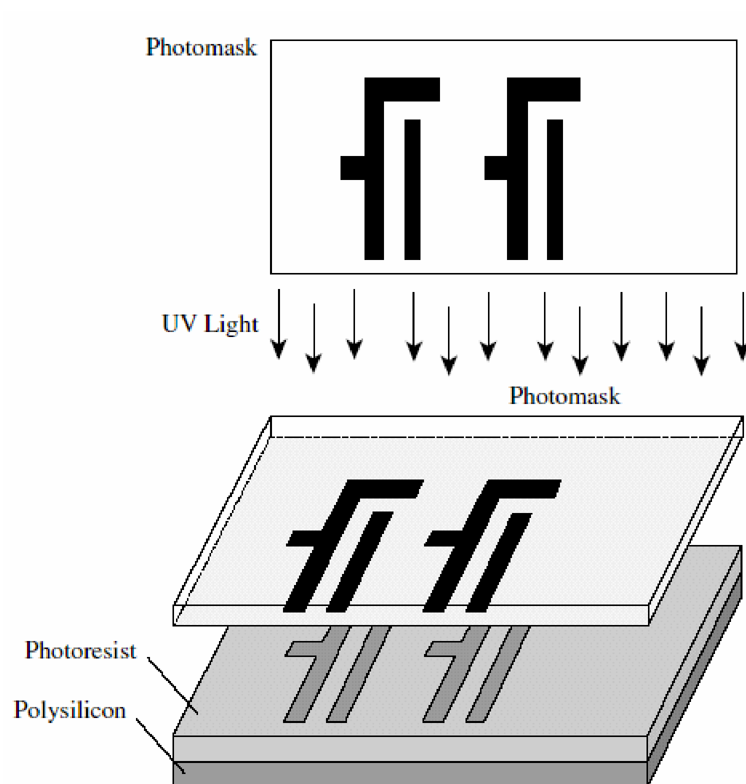
- Photoresist material
- Mask
- Material to be patterned (e.g., polysilicon)

Steps:

- Apply photoresist
- Soft bake (drives off solvents in the photoresist)
- Expose the photoresist to UV through a mask
- Develop
- Hard bake (~100°C)
- *Remove photoresist (solvents)*

The process of exposing selective areas to light through a mask is called *printing*.

- contact printing
- proximity printing
- projection printing

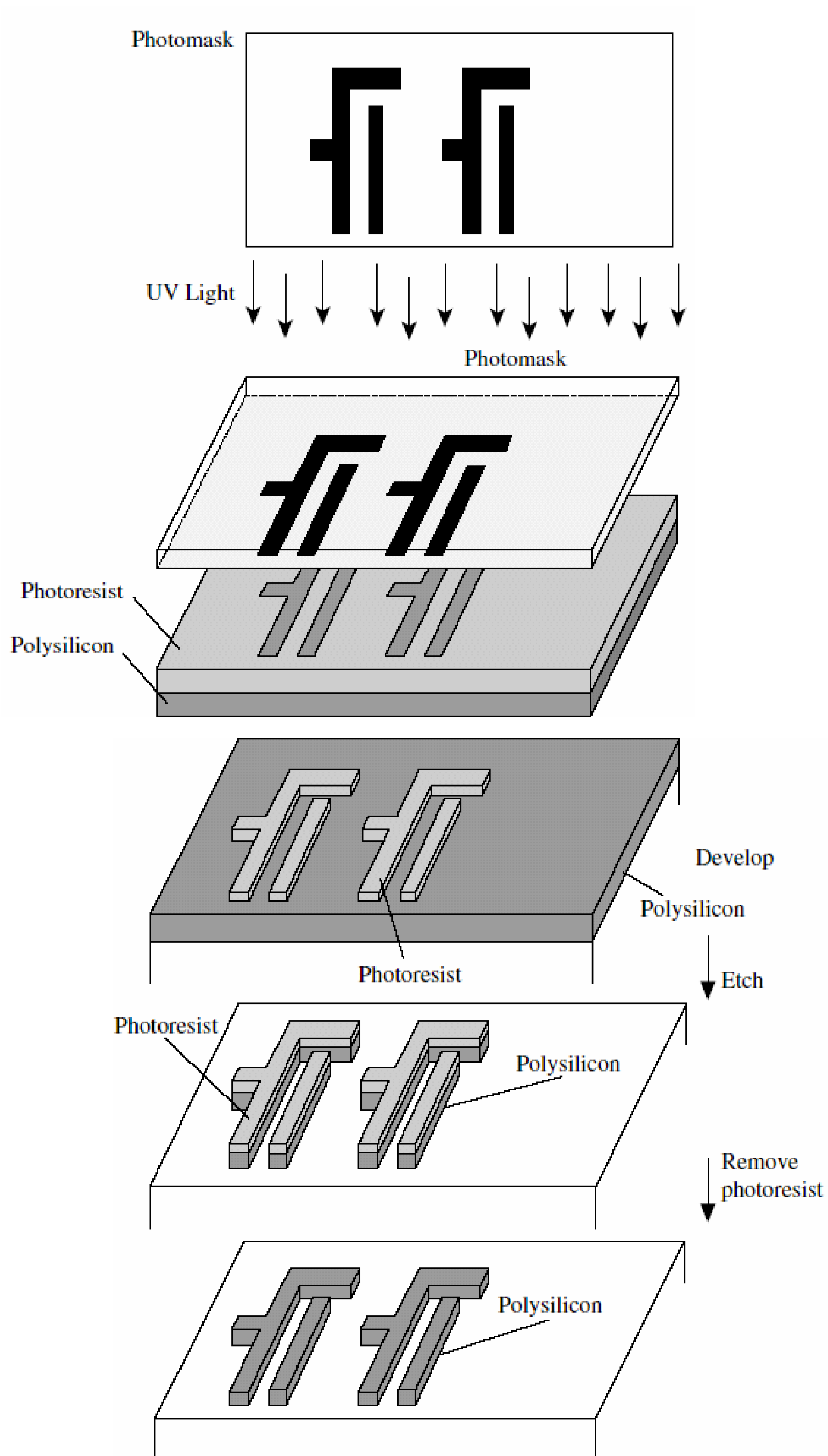


The photoresist process can be *positive*

(i.e. the pattern is the same as the mask)

or *negative* (the pattern is opposite to the mask)!!!

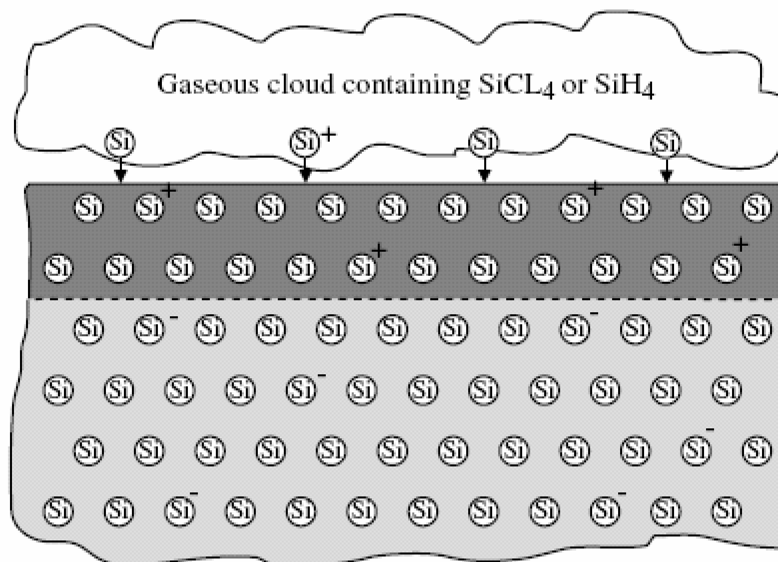
Example: positive photoresist



Epitaxy

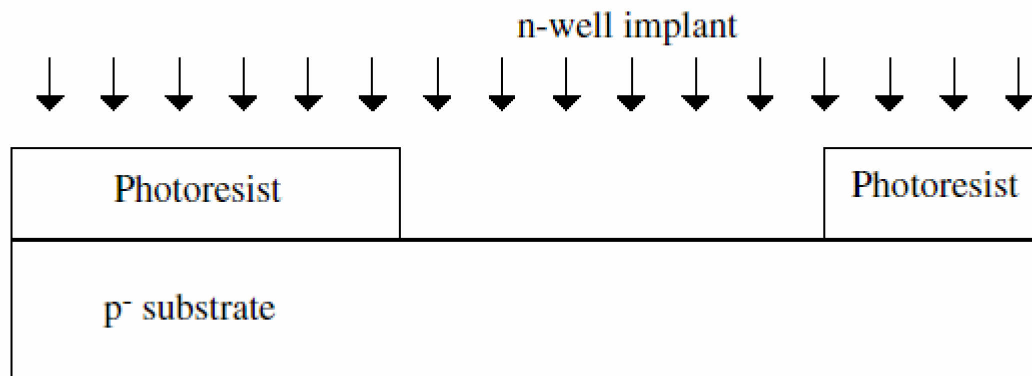
Epitaxy growth consist of the formation of a layer of a single-crystal silicon on the surface of the silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- The epitaxial layer (epi) can be doped differently, even oppositely, of the material on which if grown.
- The epi layer can be any thickness.
- The epi layer can be grown only on silicon!

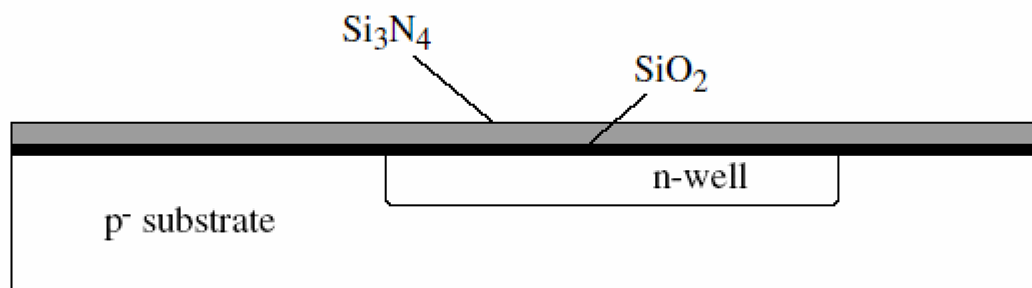


Major n-well CMOS process steps

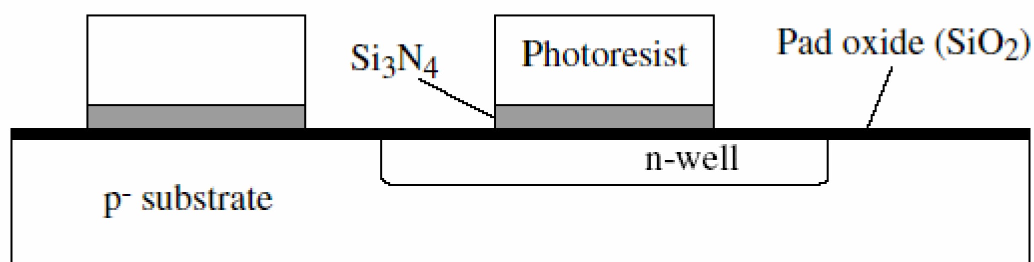
Step 1 – Implantation and diffusion of the n-wells



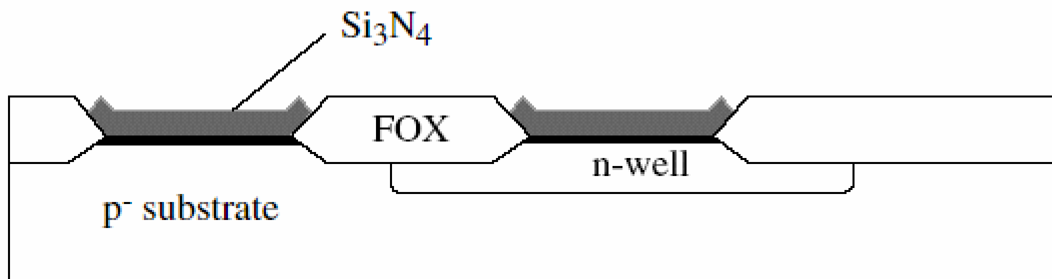
Step 2 – Growth of thin oxide and deposition of Silicon nitride



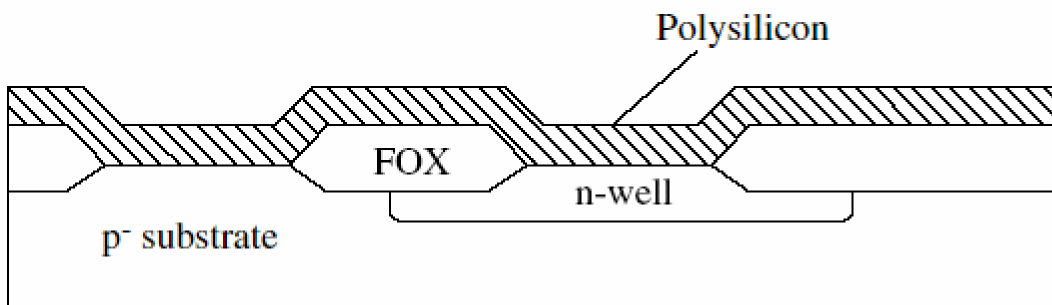
Step 3 – Selective removal of the silicon nitride



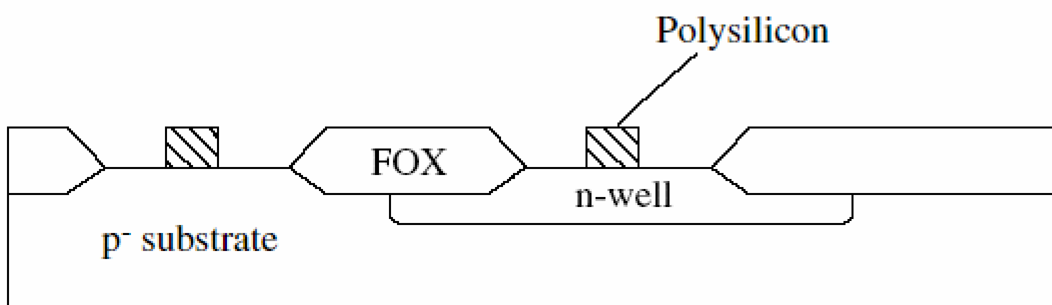
Step 4 – Growth of the thick field oxide (LOCOS – *lo*calized *o*xidation of *s*ilicon)



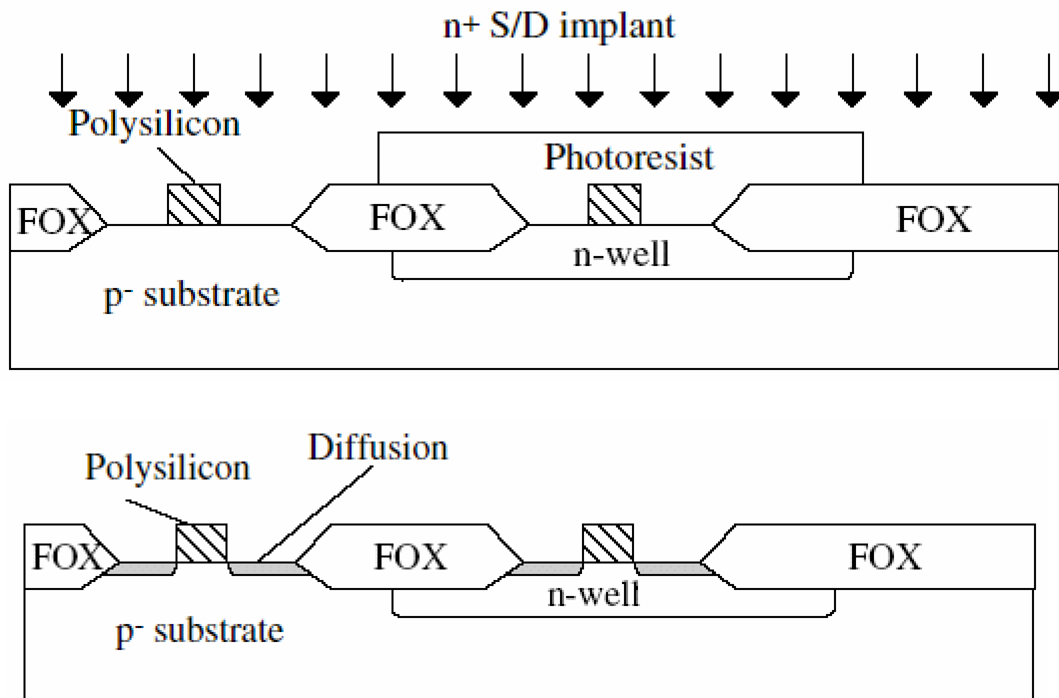
Step 5 – Removal of the nitride, growth of the thin gate oxide and deposition of polysilicon



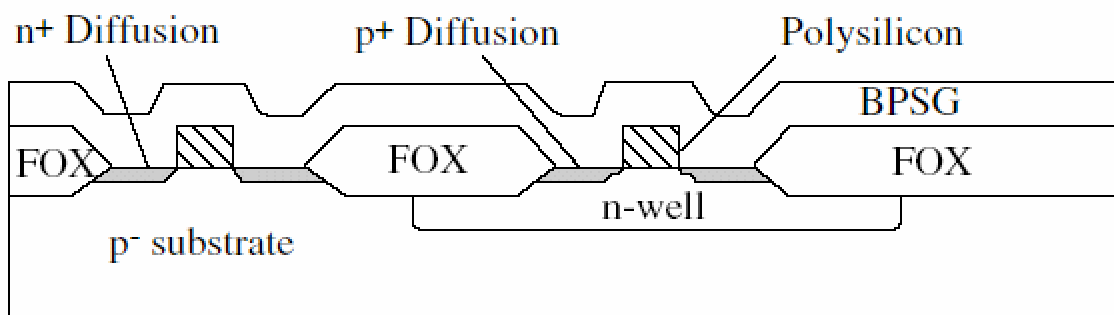
Step 6 – Selective removal of polysilicon



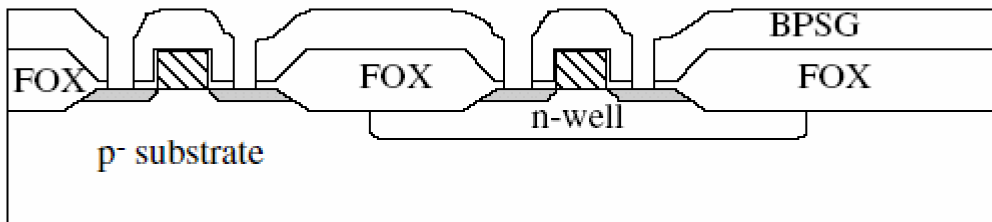
Step 7 – Implantation of the NMOS and PMOS (not shown) source and drain diffusion



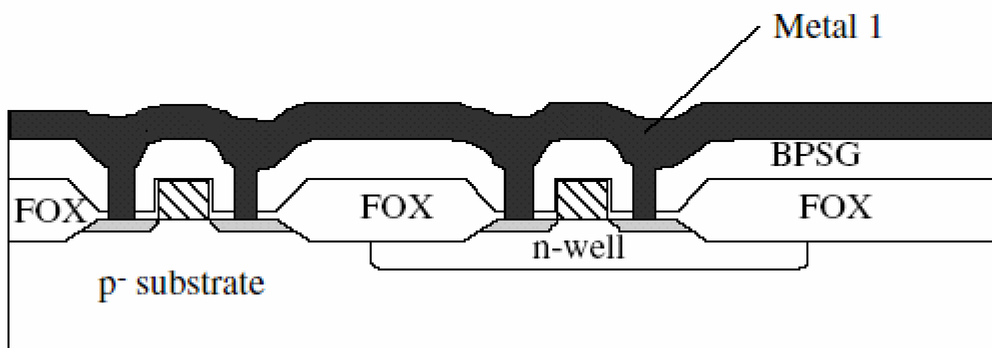
Step 8 – Deposit a thick oxide layer (BPSG – borophosphosilicate glass)



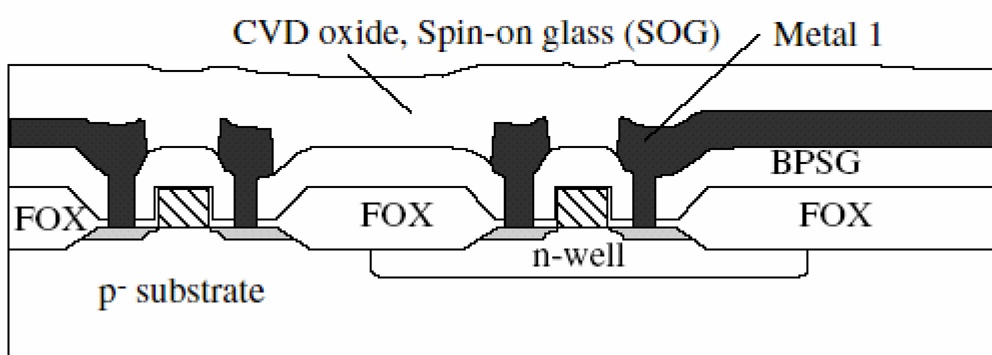
Step 9 – Open contacts,…



Step 10 – … deposit first level metal,…



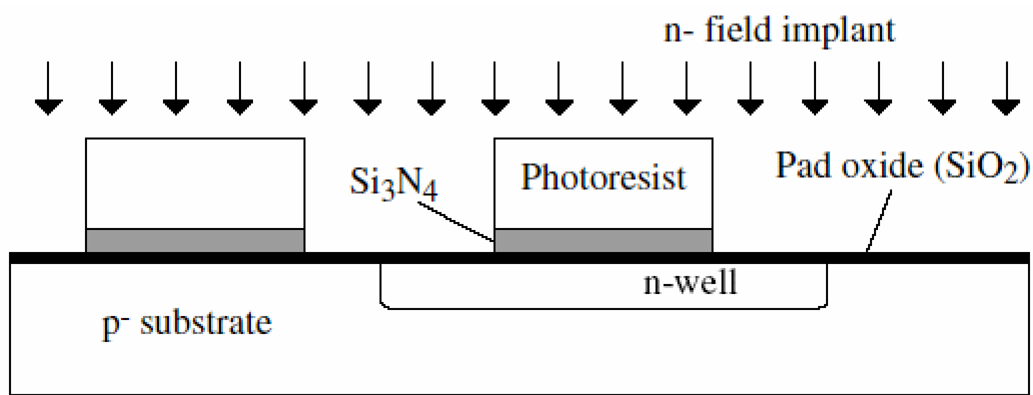
Step 11 – … etching unwanted metal and passivation



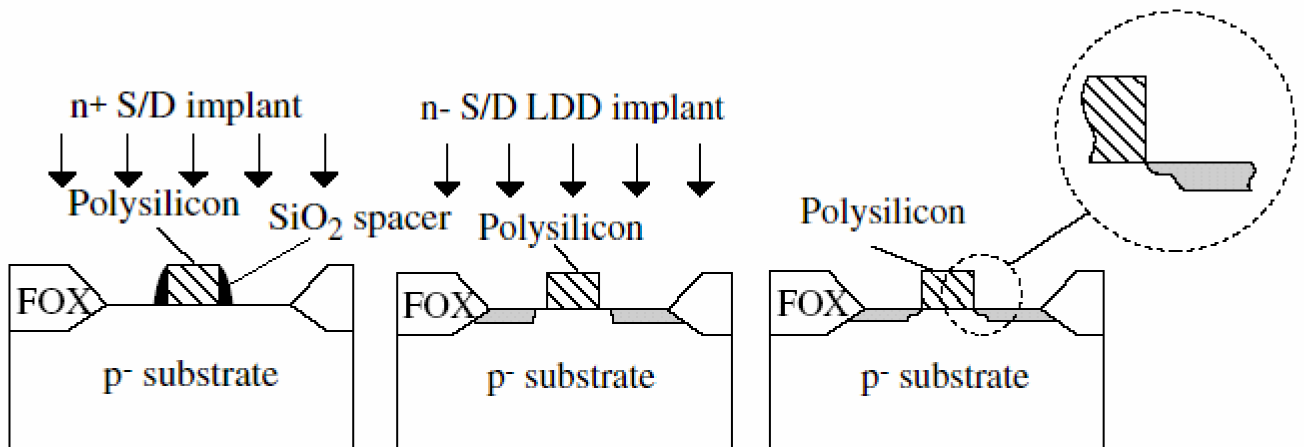
And so on…

A real process is more complex than the described one…

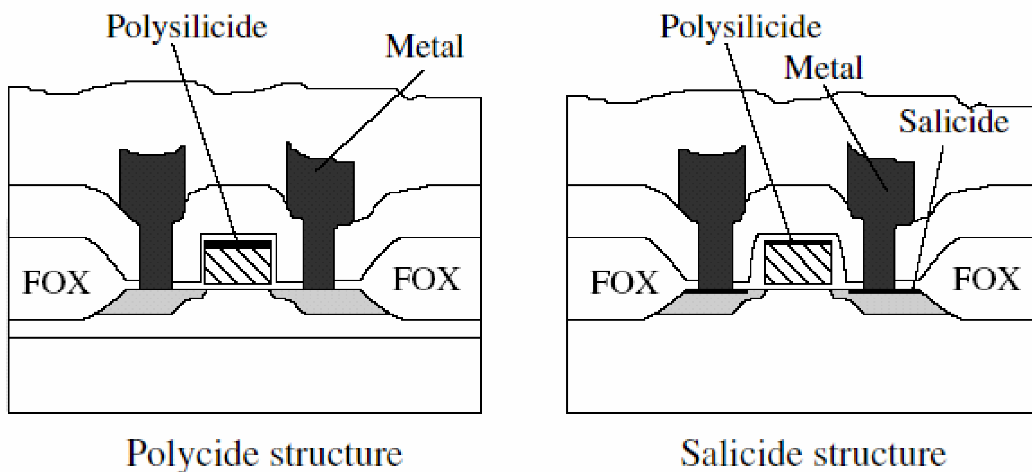
- Channel stop



- LDD process – Lightly Doped Drain

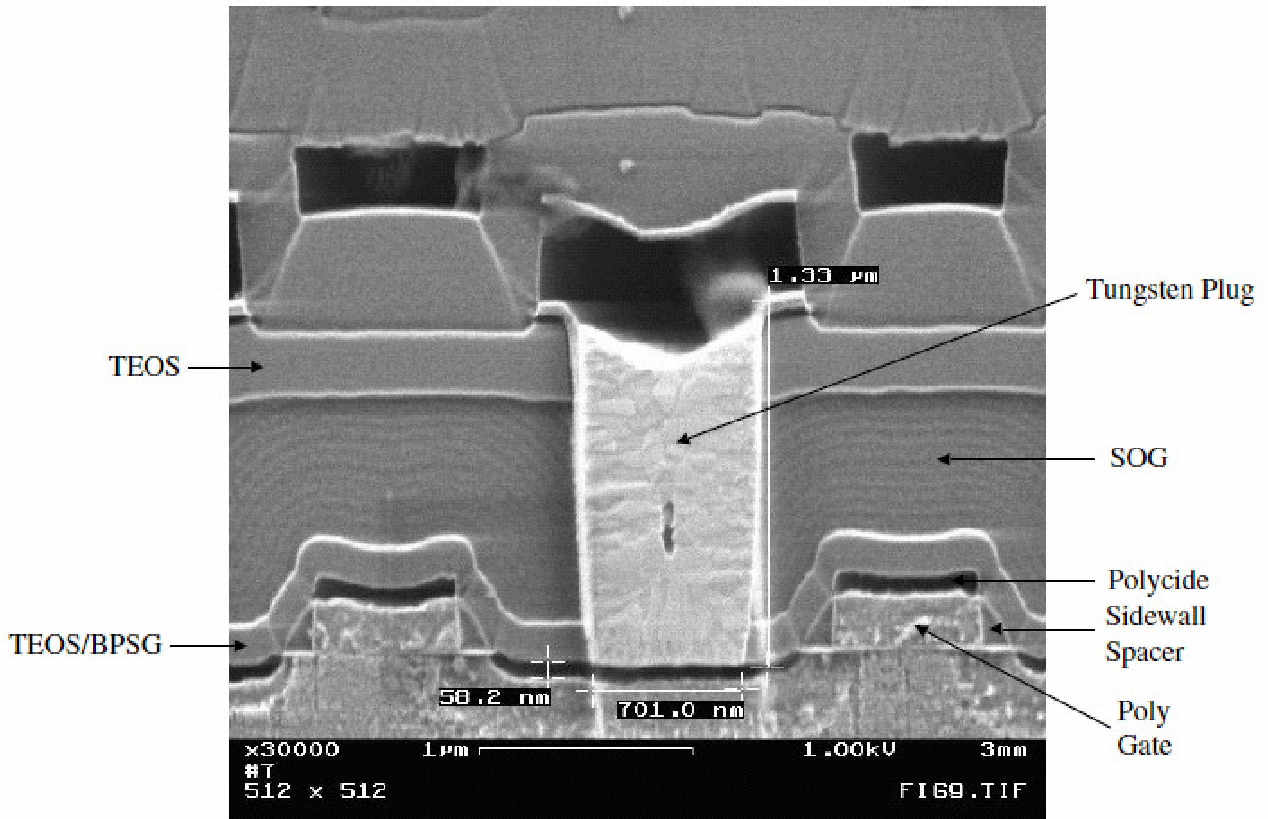


- Silicide/Salicide Technology



Polycide structure   Salicide structure

The result:



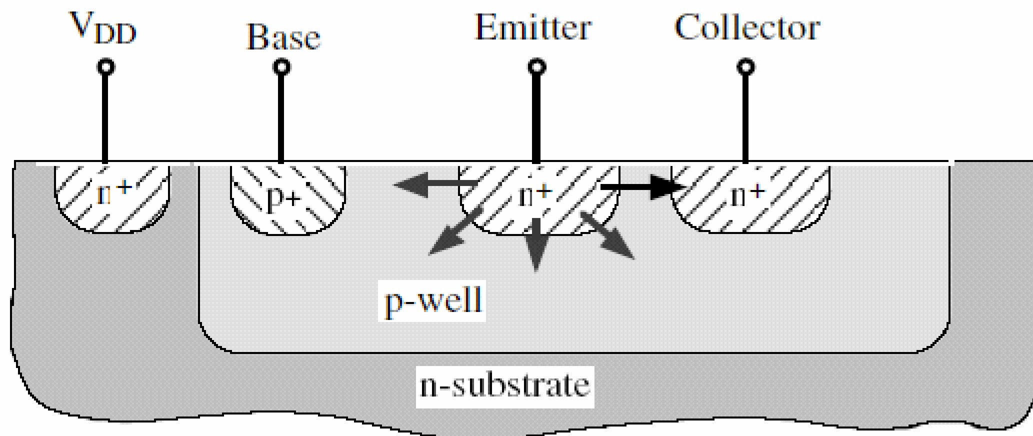
Actual CMOS trends:

- twin well / SOI
- double/triple gate
- metal gate

What about other components (BJT, resistors, capacitors)?

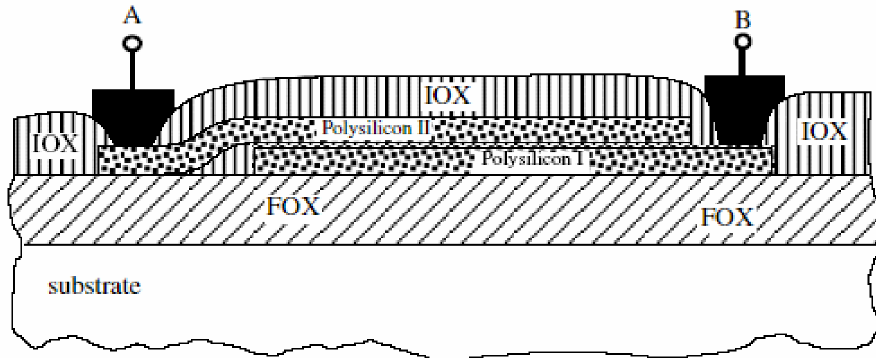
In a standard CMOS technology all BJT are parasitic lateral BJT (very low performance…)

- n-well: pnp
- p-well: npn

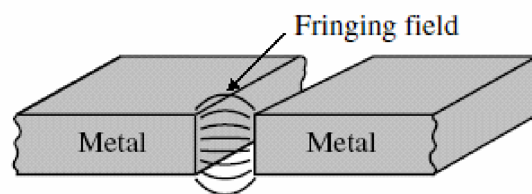


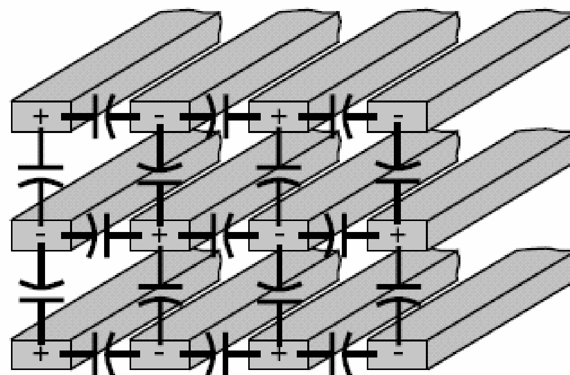
Capacitors:

- Poly1/poly2 capacitors:



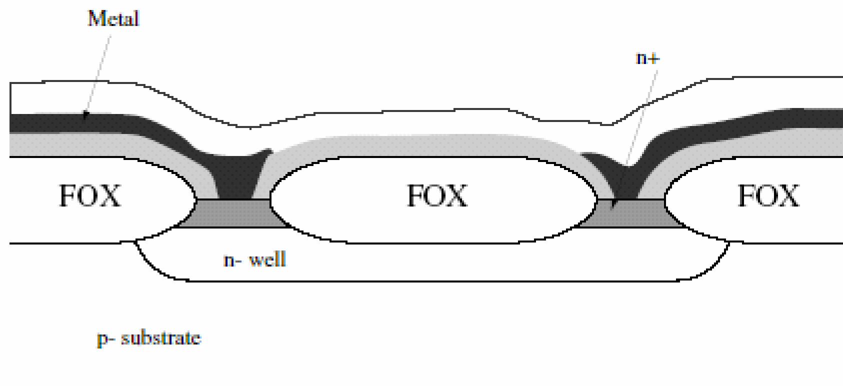
- Metal capacitors





Resistors:

- well resistors:



- Polysilicon resistors: