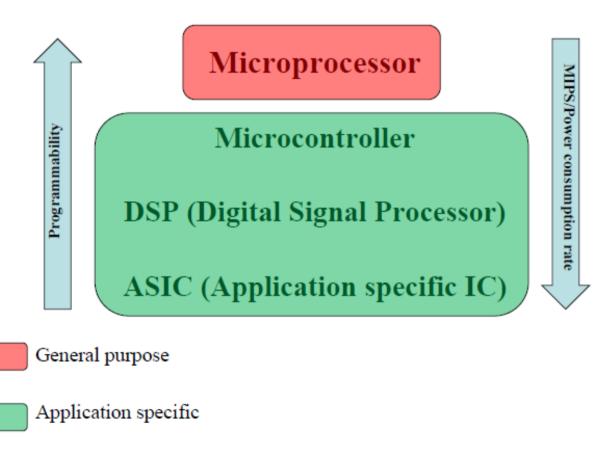
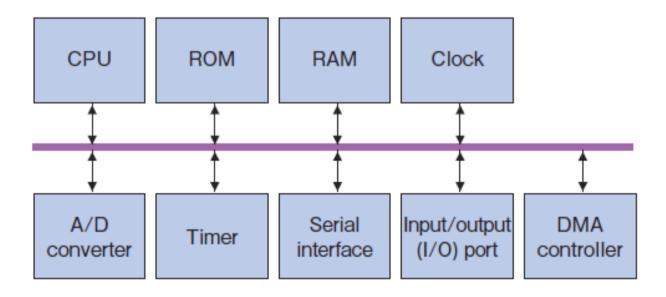
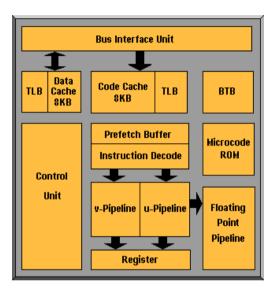
Microcontrollori

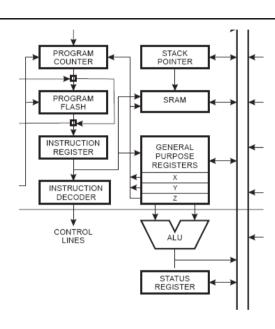


Microcontrollori



Microcontrollori – CPU





Instruction set

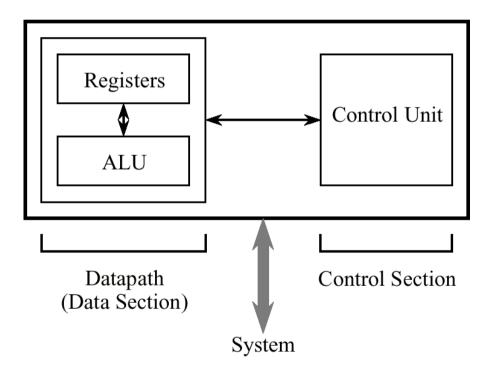
- -CISC Complex Instruction Set Computing (Intel x86 family; Motorola 680x0)
- -RISC Reduced Instruction Set computer (ARM family, ATMEL AVR Family)

Architecture (respect integer operand maximum dimension)

- -8 bit (Intel 8051, ATMEL AVR, PIC)
- -16 bit (Intel 8088, Motorola 68000, TI MSP430)
- -32 bit (x86 family, Motorola 680x0, ATMEL AVR32, Power PC)
- -64 bit (x86-64 family, Power PC)

Microcontrollori - CPU

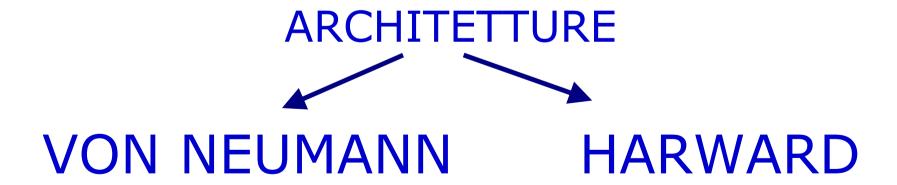
Costituita da una unità aritmetica e una unità di controllo che interpreta le istruzioni e gestisce il trasferimento dei dati nei Registri.



Microcontrollori - Architettura

Informazioni presenti in un programma:

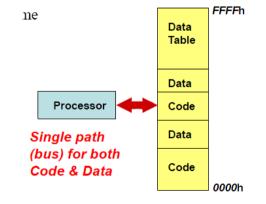
Codice di Istruzioni per l'esecuzione Dati utilizzati dalle Istruzioni



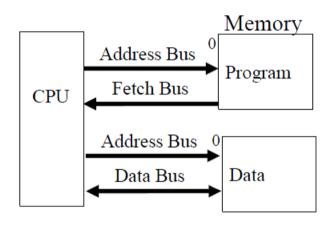
Microcontrollori - Memoria

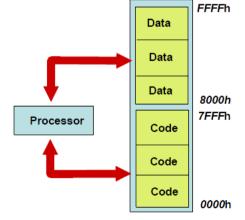
VON NEUMANN

Address Bus O Program + Data 2n



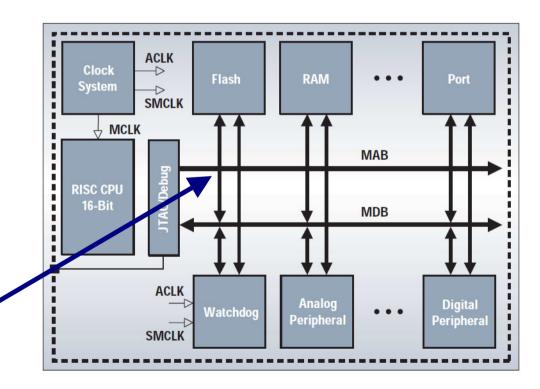
HARWARD





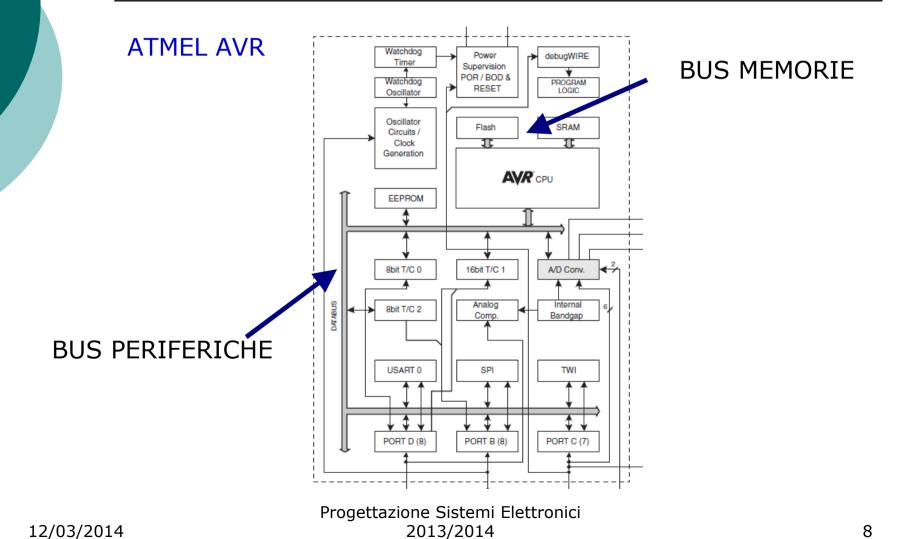
Microcontrollori - Architettura

MSP 430 TEXAS INSTRUMENT



BUS PERIFERICHE + Memorie

Microcontrollori - Architettura



Microcontrollori – Registri Interni

Registri dedicati:

Program Counter (PC):

Puntatore alla prossima istruzione che deve essere letta ed eseguita dalla CPU.

■Stack Pointer (SP):

Utilizzato per memorizzare informazioni sullo stato delle istruzioni (instructions: store by PUSH, retrieve by POP);

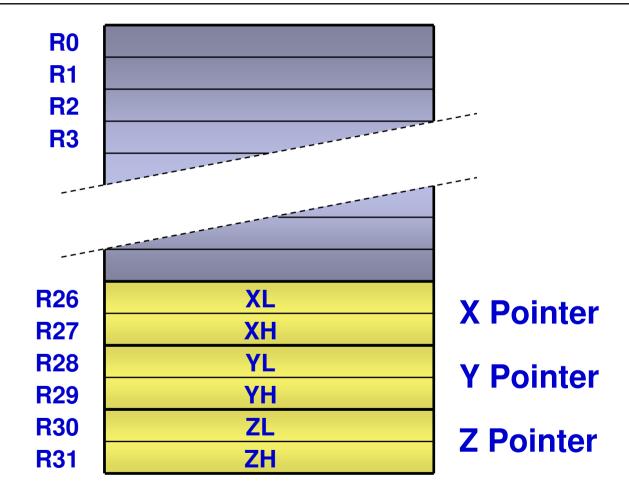
utilizzato per i parametri delle routine (PUSH, POP in calling routine)

urato dalle subroutine per memorizzare il punto di ritorno al programma (RET).

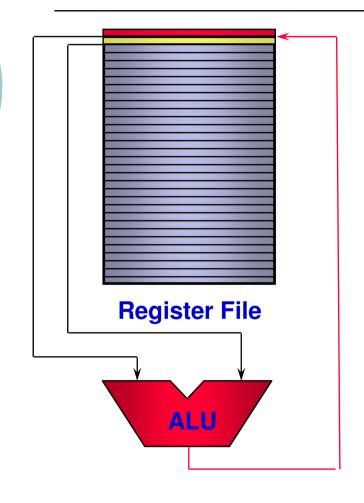
■Status Register (SR):

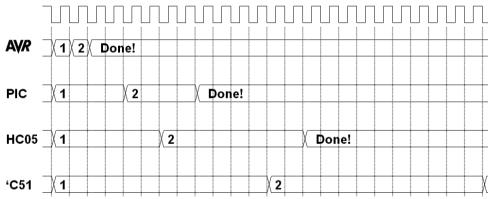
Registro di stato della CPU, aggiornato automaticamenete dalla CPU.

Microcontrollori – General Purpose Register



Microcontrollori – General Purpose Register





Microcontrollori – Processor Size

•Unità di Misura: Bits

•Corrisponde alla dimensione massima dei dati che può elaborare la CPU

•Rispecchia la dimensione del bua interno e della memoria die registri della CPU

•Architetture standard: 8, 16, 32 Bits

Microcontrollori- Performance Metrics

Elaborazione:

- Clock Speed
- MIPS (instructions per sec)
- Latency
- Throughput

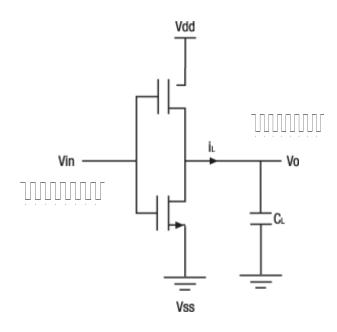
Elettrciche:

- Power Consumptions
- Voltage Supply
- Noise Immunity
- Sensitivity

Contributi al consumo di potenza nei dispositivi CMOS:

- Consumo dinamico (P_{DYN})
- •Consumo di corto circuito (P_{SHORT})
- •Consumi di Leakage (P_{LEAK})

$$P = P_{DYN} + P_{SHORT} + P_{LEAK}$$



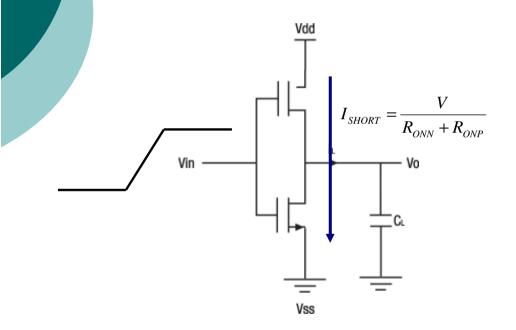
$$P_{DYN} = A \cdot C \cdot V^2 \cdot f$$

A: Attività del Gate

C: Capacità di carico

V: Tensione di alimentazione

f: Frequenza del clock



$$P_{SHORT} = \tau \cdot A \cdot V \cdot I_{SHORT} \cdot f$$

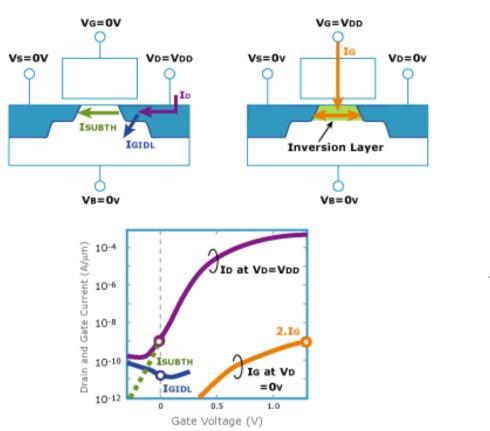
t=Tempo di corto circuito

A: Attività del Gate

 I_{SHORT} : Corrente di corto circuito

V: Tensione di alimentazione

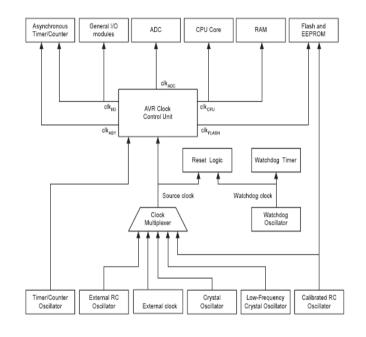
f: Frequenza del clock

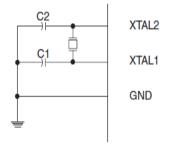


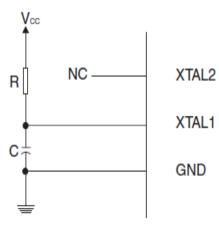
$$P_{LEAK} = V \cdot I_{LEAK}$$

	Active Clock Domains			Oscillators		Wake Up Sources							
Sleep Mode	clk _{CPU}	clk _{FLASH}	clk _{IO}	clk _{ADC}	clk _{ASY}	Main Clock Source Enabled	Timer Osc Enabled	INT7:0	TWI Address Match	Timer 0	SPM/ EEPROM Ready	ADC	Other I/O
Idle			Χ	Х	Х	Х	X ⁽²⁾	Х	Х	Х	Х	Χ	Х
ADC Noise Reduction				Х	Х	х	X ⁽²⁾	X ⁽³⁾	Х	х	Х	Х	
Power- down								X ⁽³⁾	Х				
Power- save					X ⁽²⁾		X ⁽²⁾	X ⁽³⁾	Х	X ⁽²⁾			
Standby ⁽¹⁾						Х		X ⁽³⁾	Х				
Extended Standby ⁽¹⁾					X ⁽²⁾	Х	X ⁽²⁾	X ⁽³⁾	Х	X ⁽²⁾			

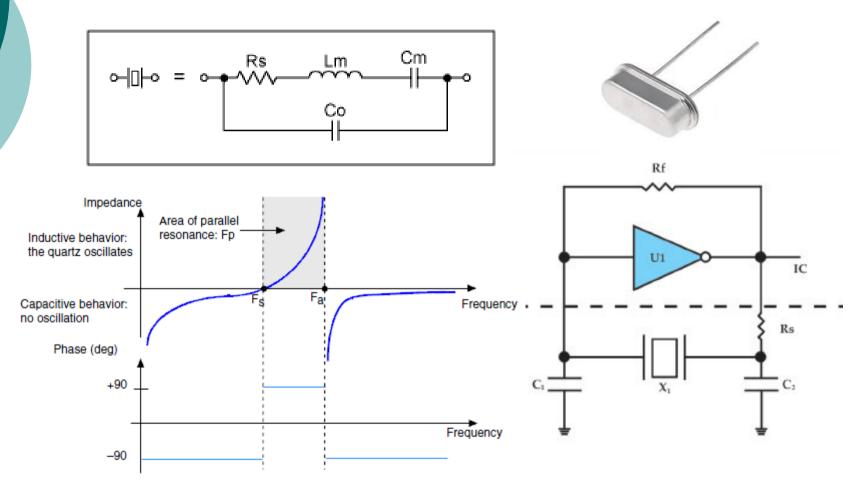
Microcontrollori – Clock System







Microcontrollori - Crystal



Microcontrollori - Crystal

Specifiche:

Quality Factor

Rapporto fra l'energia immagazzinata e quella dissipata . Q alto → lentezza nella partenza Load Capacitance

Capacità necessaria per far oscillare il quarzo ESR

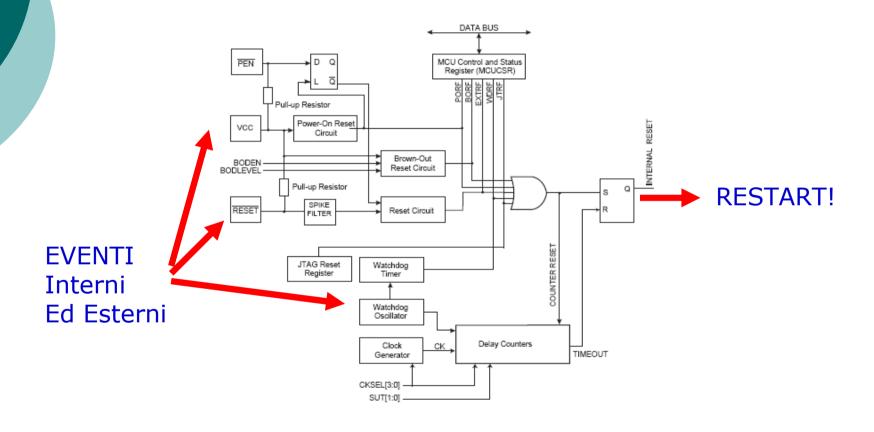
Resistenza serie equivalente

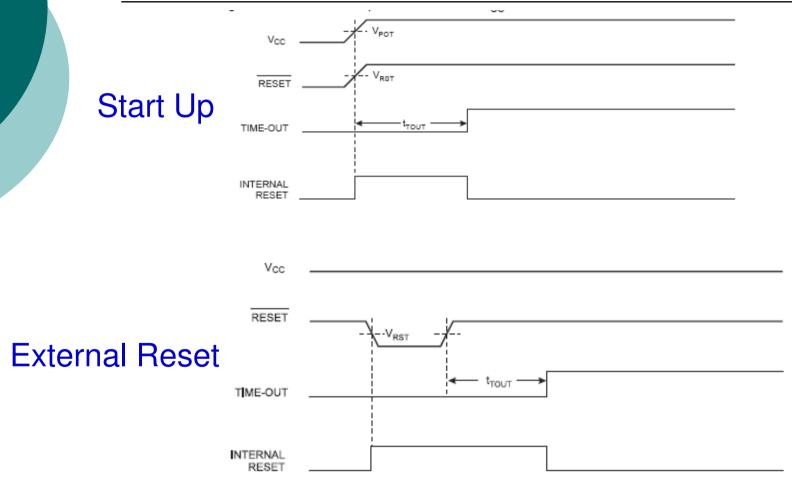
Frequency Stability

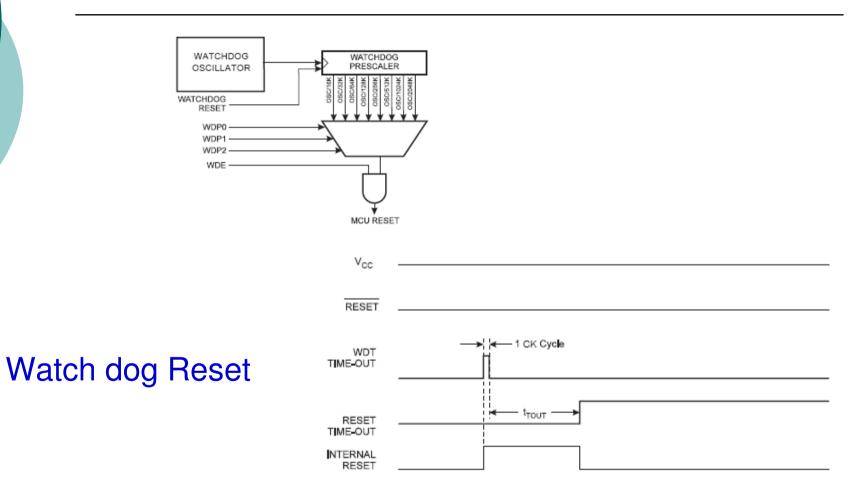
Massima deviazione della frequenza dalla specifica in un dato range di temperatura

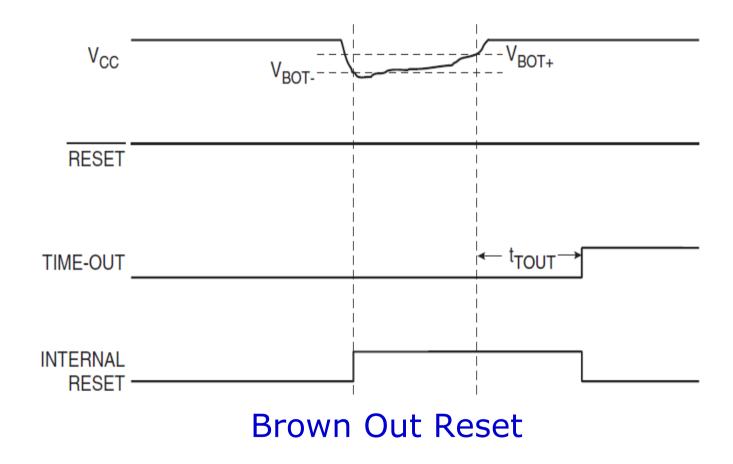
Frequency Tolerance

Massima deviazione della frequenza dalla specifica a 25° C.





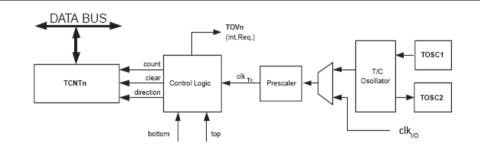


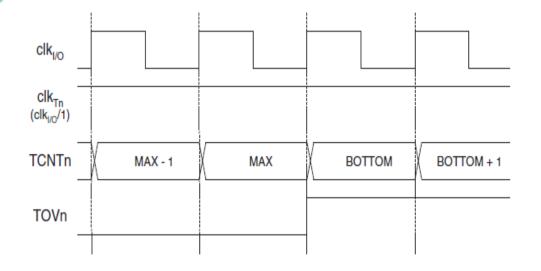


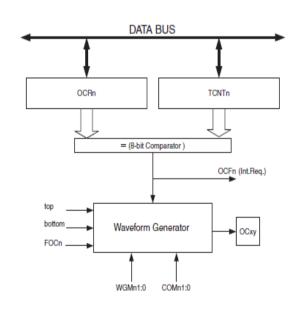
In quale stato riporta il dispositivo?

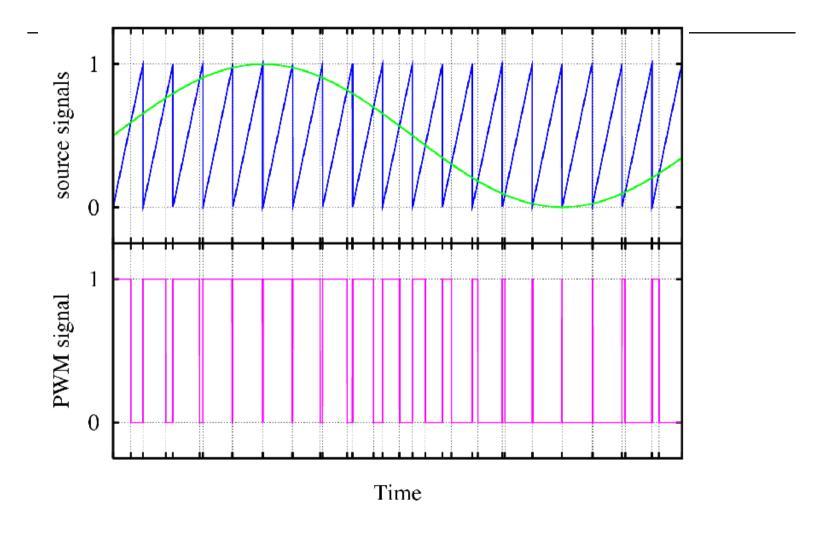
	Power-On Reset	External Reset	Watchdog Reset	BOD Reset	BOD33 Reset	CPU Error Reset	OCD Reset
CPU/HSB/PBA/PBB (excluding Power Manager)	Y	Y	Y	Y	Y	Y	Y
32 KHz oscillator	Υ	N	N	N	N	N	N
RTC control register	Υ	N	N	N	N	N	N
GPLP registers	Y	N	N	N	N	N	N
Watchdog control register	Υ	Y	N	Υ	Υ	Y	Y
Voltage calibration register	Y	N	N	N	N	N	N
RCSYS Calibration register	Υ	N	N	N	N	N	N
BOD control register	Υ	Y	N	N	N	N	N
BOD33 control register	Y	Y	N	N	N	N	N
Bandgap control register	Υ	Y	N	N	N	N	N
Clock control registers	Y	Y	Y	Y	Y	Y	Y
Osc0/Osc1 and control registers	Y	Y	Υ	Υ	Y	Y	Y
PLL0/PLL1 and control registers	Y	Y	Y	Y	Y	Y	Y
OCD system and OCD registers	Y	Y	N	Y	Y	Y	N

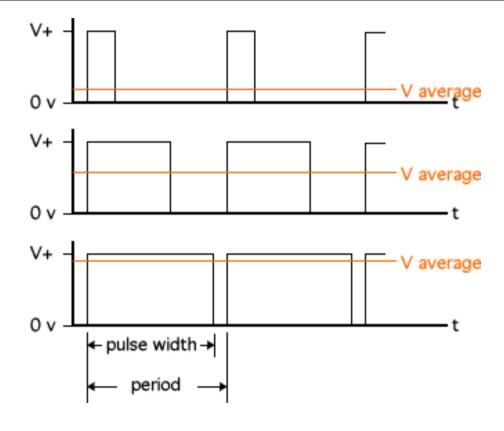
Microcontrollori - Timer

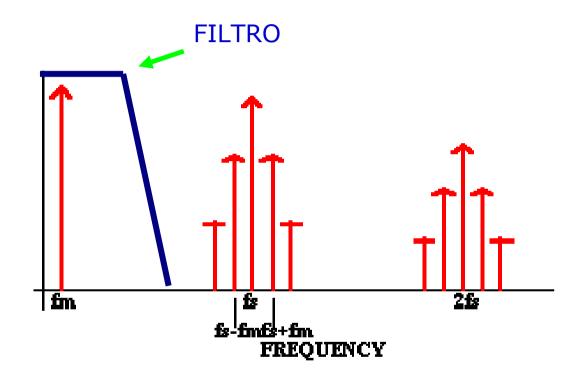


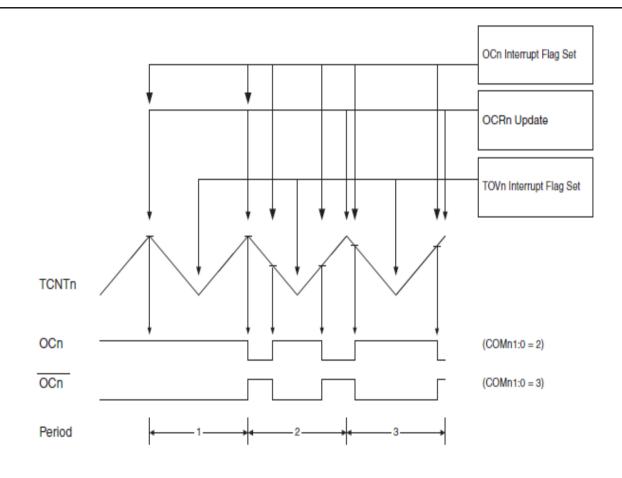








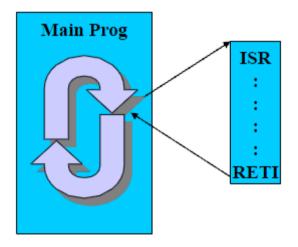




Microcontrollori - Interrupt

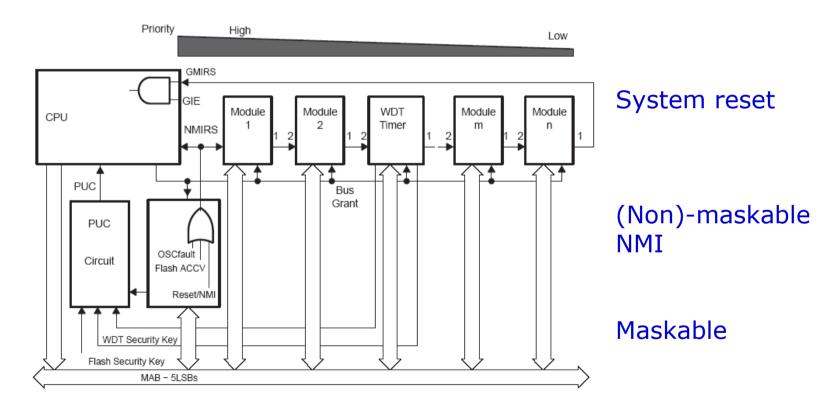
Permette di rispondere ad un evento "Esterno" senza polling

"Esterno": tutto ciò che è al di fuori del Core e tutto ciò che può attivare i flag di interrupt



Microcontrollori - Interrupt

Figure 2-4. Interrupt Priority



Microcontrollori - Interrupt

Vector No.	Program Address ⁽²⁾	Source	Interrupt Definition
1	\$0000 ⁽¹⁾	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	\$0002	INT0	External Interrupt Request 0
3	\$0004	INT1	External Interrupt Request 1
4	\$0006	INT2	External Interrupt Request 2
5	\$0008	INT3	External Interrupt Request 3
6	\$000A	INT4	External Interrupt Request 4
7	\$000C	INT5	External Interrupt Request 5
8	\$000E	INT6	External Interrupt Request 6
9	\$0010	INT7	External Interrupt Request 7
10	\$0012	TIMER2 COMP	Timer/Counter2 Compare Match
11	\$0014	TIMER2 OVF	Timer/Counter2 Overflow
12	\$0016	TIMER1 CAPT	Timer/Counter1 Capture Event
13	\$0018	TIMER1 COMPA	Timer/Counter1 Compare Match A
14	\$001A	TIMER1 COMPB	Timer/Counter1 Compare Match B
15	\$001C	TIMER1 OVF	Timer/Counter1 Overflow
40	A004E	TILLEDA GOLLO	T

Address	LabelsCode		C	omments
\$0000	jmp	RESET	;	Reset Handler
\$0002	jmp	EXT_INT0	;	IRQ0 Handler
\$0004	jmp	EXT_INT1	;	IRQ1 Handler
\$0006	jmp	EXT_INT2	;	IRQ2 Handler
\$0008	jmp	EXT_INT3	;	IRQ3 Handler
\$000A	jmp	EXT_INT4	;	IRQ4 Handler
\$000C	jmp	EXT_INT5	;	IRQ5 Handler
\$000E	jmp	EXT_INT6	;	IRQ6 Handler
\$0010	jmp	EXT_INT7	;	IRQ7 Handler
\$0012	jmp	TIM2_COMP	;	Timer2 Compare Handler
\$0014	jmp	TIM2_OVF	;	Timer2 Overflow Handle
\$0016	jmp	TIM1_CAPT	;	Timer1 Capture Handler
\$0018	jmp	TIM1_COMPA	Α;	Timer1 CompareA Handle
\$001A	jmp	TIM1_COMP	3;	Timer1 CompareB Handle
\$001C	jmp	TIM1_OVF	;	Timer1 Overflow Handle
\$001E	jmp	TIM0_COMP	;	Timer0 Compare Handler
\$0020	jmp	TIMO_OVF	;	Timer0 Overflow Handle

Microcontrollori - Interrupt Overheads

Interrupt arrives
Complete current instruction
Save essential register information
Vector to ISR
Save additional register information

Interrupt Latency

Execute body of ISR

Restore other register information
Return from interrupt and restore essential
registers
Resume task

Interrupt Termination

